IN THE CLAIMS

Please AMEND claim 11.

Please ADD new claims 32-36 in accordance with the following.

1. (ORIGINAL) An interface having a plug and play function and connected to a host controller, wherein the interface performs a predetermined bus reset sequence in response to a bus reset generated by the plug and play function in accordance with a change in the status of an external bus, the interface comprising:

an analysis circuit for analyzing data provided from the external bus during the bus reset sequence and for determining whether the bus reset sequence has been completed normally, wherein the analysis circuit provides the data to the host controller when the bus reset sequence has been completed normally.

2. (ORIGINAL) An interface system having a plug and play function and connected to a host controller, wherein the interface system performs a predetermined bus reset sequence in response to a bus reset generated by the plug and play function in accordance with a change in the status of -an external bus, the interface system comprising:

an analysis circuit for analyzing data provided from the external bus during the bus reset sequence and determining whether the bus reset sequence has been completed normally, wherein the analysis circuit provides the data to the host controller when the bus reset sequence has been completed normally.

3. (ORIGINAL) The interface system according to claim 2, wherein the analysis circuit generates the bus reset upon detecting an abnormality of the data during the data analysis.

4. (ORIGINAL) The interface system according to claim 2, wherein the analysis circuit generates the bus reset upon detecting an abnormality of the data during the data analysis after providing the host controller with one of an interrupt event and necessary data.

5. (ORIGINAL) The interface system according to claim 2, wherein the analysis circuit provides the host controller with necessary data.

6. (ORIGINAL) The interface system according to claim 2, further comprising a buffer memory connected to the analysis circuit for storing the data provided from the external bus.

7. (ORIGINAL) The interface system according to claim 6, wherein the analysis circuit stores the data in the buffer memory and simultaneously analyzes the data.

8. (ORIGINAL) The interface system according to claim 6, wherein the analysis circuit analyzes the data stored in the buffer memory after storing the data in the buffer memory and after completion of the bus reset sequence.

9. (ORIGINAL) The interface system according to claim 2, wherein the data includes a packet provided from an external node via the external bus in the bus reset sequence, and the analysis circuit analyzes the packet to determine whether the external bus is functioning normally.

10. (ORIGINAL) The interface system according to claim 2, wherein the data includes information indicating a change in the status of the external bus, and the analysis circuit

determines whether the information corresponds to the bus reset sequence.

11. (CURRENTLY AMENDED) The interface system according to claim 2, further comprising:

a port circuit for detecting the status of the external bus and generating associated detection information;

a physical layer circuit connected to the port circuit to receive the data via the port circuit and generate a data packet;

a link layer circuit connected to the physical layer circuit to determine whether the data packet is addressed to the interface system; and

a buffer memory connected to the link layer circuit to store the detection information and the data packet which are provided via the port circuit, the physical layer circuit, and the link layer circuit, wherein the analysis circuit includes,

a first analysis circuit connected to the port circuit to analyze the detection information, and

a second analysis circuit connected to the physical layer circuit to analyze the data packet provided during the bus reset sequence and to determine whether the data packet is normal, wherein the analysis circuit determines whether the bus reset sequence has been completed normally based on the analysis result of the first and the second analysis circuits.

12. (ORIGINAL) The interface system according to claim 11, wherein the first analysis circuit compares the detection Information with predetermined sequence information, the second analysis circuit compares the data packet with a predetermined data packet, and the analysis circuit determines whether the bus reset sequence has been completed normally based on the comparison result of the first and the second analysis circuits.

13. (ORIGINAL) An interface that performs a predetermined connection procedure with a network, the interface comprising:

a self-diagnosis circuit for performing self-diagnosis of the interface prior to the predetermined connection procedure, wherein the interface suspends transition to the predetermined connection procedure when the self-diagnosis circuit generates a diagnosis indicating an abnormality of the interface.

14. (ORIGINAL) The interface according to claim 13, wherein the self-diagnosis circuit determines whether the status of the interface satisfies a predetermined self-diagnosis initiation requirement and initiates the self-diagnosis when the self-diagnosis initiation requirement is satisfied.

15. (ORIGINAL) The interface according to claim 13, wherein the predetermined connection procedure includes a bus reset sequence.

16. (ORIGINAL) The interface according to claim 13, wherein the interface stops the operation of the interface and suspends transition to the predetermined connection procedure when

the interface has an abnormality.

17. (ORIGINAL) The interface according to claim 13, wherein the interface continues to perform the self-diagnosis of the interface after performing the predetermined connection procedure, and the interface stops operation of at least a part of the interface that

does not transfer data with the network when the self-diagnosis circuit generates a diagnosis indicating an abnormality of the interface.

18. (ORIGINAL) The interface according to claim 13, wherein the self-diagnosis circuit generates information when the interface has an abnormality, the information indicating the location of the abnormality.

19. (ORIGINAL) The interface according to claim 13, further comprising a data transfer control circuit for performing the predetermined connection procedure and transferring data with the network, the data transfer control circuit including;

a plurality of ports connected to the network and including a first port and a second port;

a transmitting circuit connected to the plurality of ports; and

a receiving circuit connected to the plurality of ports,

wherein the self-diagnosis circuit connects the first port and the second port to each other and tests the data transfer control circuit using the data transferred from the transmitting circuit to the receiving circuit via the first and second ports.

20. (ORIGINAL) The interface according to claim 19, wherein the self-diagnosis circuit includes:

a self-diagnosis control circuit for determining whether the status of the interface satisfies a predetermined self-diagnosis initiation requirement, wherein the self-diagnosis control circuit generates a self-diagnosis initiation signal and performs self-diagnosis when the predetermined self-diagnosis initiation requirement is satisfied; and

a connection control circuit connected to the self-diagnosis control circuit to connect the first and second ports to each other in response to the self-diagnosis initiation signal.

21. (ORIGINAL) The interface according to claim 20, wherein the self-diagnosis control circuit includes:

a self-diagnosis initiation detection circuit for generating the self-diagnosis initiation signal when the self-diagnosis initiation requirement is satisfied;

a shift control circuit connected to the data transfer control circuit and the self-diagnosis initiation detection circuit, wherein the shift control circuit shifts the data transfer control circuit from a data transfer mode to a self-diagnosis mode;

a data generation circuit connected to the data transfer control circuit and the self-

diagnosis .initiation detection circuit, wherein the data generation circuit generates diagnosis data used to test the data transfer control circuit in response to the self-diagnosis initiation signal and provides the diagnosis data to the data transfer control circuit; and

a transfer data comparator connected to the data transfer control circuit and the data generation circuit, wherein the transfer data comparator compares the diagnosis data with the data transferred from the data transfer control circuit.

22. (ORIGINAL) The interface according to claim 21, wherein the data transfer control circuit includes a plurality of registers, wherein the data generation circuit stores predetermined register data in the plurality of registers, and wherein the self-diagnosis circuit further includes a register data comparator for comparing the register data and the data provided from the data transfer control circuit and read from the plurality of registers.

23. (ORIGINAL) The interface according to claim 19, wherein the testing of the data transfer control circuit includes at least one of a direct current characteristic test of the plurality of ports, an alternating current characteristic test of the plurality of ports, and a data transfer test of the data transfer control circuit.

24. (ORIGINAL) A self-diagnosis method employed by an interface that performs a predetermined connection procedure with a network, wherein the interface has a plurality of ports, a transmitting circuit, and a receiving circuit, the plurality of, ports including a first port and a second port, and the transmitting and receiving circuit each being connected to the plurality of ports, the self-diagnosis method comprising the steps of:

connecting the first and second ports to each other prior to the predetermined connection procedure;

transferring data from the transmitting circuit to the receiving circuit via the first and second ports; and

comparing data transmitted by the transmitting circuit and data received by the receiving circuit.

25. (ORIGINAL) The self-diagnosis method according to claim 24, further comprising the step of:

testing a direct current characteristic of the plurality of ports by transferring direct current signals between the first and second ports.

26. (ORIGINAL) The self-diagnosis method according to claim 24, further comprising the step of:

testing an alternating current characteristic of the plurality of ports by transferring direct current signals between the first and second ports.

27. (ORIGINAL) The self-diagnosis method according to claim 24, further comprising the step of:

determining whether the status of the interface satisfies a predetermined self-diagnosis initiation requirement, wherein the connecting step is performed when the self-diagnosis initiation requirement is satisfied.

28. (ORIGINAL) The self-diagnosis method according to claim 24, wherein the predetermined connection procedure includes a bus reset sequence.

29. (ORIGINAL) The self-diagnosis method according to claim 24, further comprising the steps of:

determining whether the interface has an abnormality based on a result of the comparing step; and

suspending transition to the predetermined connection procedure when the interface is determined to have an abnormality.

30. (ORIGINAL) The self-diagnosis method according to claim 29, further comprising the step of:

generating information when the interface has an abnormality, the information indicating the location of the abnormality.

31. (ORIGINAL) The self-diagnosis method according to claim 24, further comprising the steps of:

detecting whether the network has an abnormality after the predetermined connection procedure is performed;

performing the connecting step, the transferring step, and the comparing step when an abnormality of the network is detected;

determining whether the interface has an abnormality based on a result of the

comparing step; and

stopping operation of a part of the interface that does not transfer data with the network when the interface is determined to have an abnormality.

32. (NEW) A method for transferring data comprising:

detecting a bus reset in accordance with a change in the status of a bus;

analyzing data provided from the bus during a bus reset sequence;

determining whether the bus reset sequence has been performed normally; and

transferring the data to a host controller when the bus reset sequence has been performed normally.

33. (NEW) A self-diagnosis method employed by an interface having a transmitting circuit and a receiving circuit, the self-diagnosis method comprising:

connecting the transmitting circuit and the receiving circuit to each other prior to a predetermined connection procedure;

transferring data from the transmitting circuit to the receiving circuit; and

comparing the received data with the transmitted data.

34. (NEW) The self-diagnosis method according to claim 33, further comprising suspending transition to the predetermined connection procedure based on the result of the comparing.

35. (NEW) A self-diagnosis method employed by an interface having a transmitting circuit and a receiving circuit, the self-diagnosis method comprising:

connecting the transmitting circuit and the receiving circuit to each other prior to a predetermined connection procedure; and

testing a direct current characteristic or an alternating current characteristic by transferring direct current signals between the transmitting circuit and the receiving circuit in case of the direct current characteristic test, or transferring a data signal whose waveform is same as that of data used during actual data transfer between the transmitting and receiving circuits in case of the alternating current characteristic test.

36. (NEW) The self-diagnosis method according to claim 35, further comprising suspending transition to the predetermined connection procedure based on the result of the testing.